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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,769	09/23/2003	Kenneth R. Smits	42P11022C	4381

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,769	SMITS, KENNETH R.	
	Examiner	Art Unit	
	Midys Inoa	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

TW

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/27/04 have been fully considered but they are not persuasive.

Regarding Claim 1, applicant argues that Kronstadt's single mention of redundant memory banks does not anticipate the use of redundant arrays. However, Kronstadt clearly states that an advantage of having multiple memory banks is that one or more of these memory banks can be redundant (Col. 4, lines 39-45). Although this is a short mention of redundant memory banks, it serves as anticipatory evidence and allows the examiner to interpret the Kronstadt reference disclosing as a system in which one ore more of the memory banks can be redundant.

Regarding Claims 7 and 12, applicant argues that the reference simply describes determining if there is valid data in the buffers. However, Kronstadt disclose valid fields representing the valid state of an entire bank. Additionally, it discloses instances where invalid banks are identified prior to an access and the access of the invalid bank is avoided. In this system, the invalid bank can be avoided by disabling the data line to such bank. In this case, the data line is not affected, but its connection to the invalid bank may be discontinued (Column 3, lines 15-45 and Column 4, lines 6-14). This is demonstrated by the instance in which banks are labeled invalid and a cache miss occurs until the banks are labeled valid again. The system avoids access to invalid banks.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 7, 9, and 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kronstadt et al. (4,725,945).

Regarding Claim 1, Kronstadt teaches a memory 12 (Figure 4) comprising: a plurality of arrays of memory cells (memory banks 1- n), the arrays being arranged in banks, each bank including regular arrays (array of static column mode dynamic random access memories, Column 2, lines 11-28) and a redundant array (supports one or more redundant memory banks, Column 4, lines 25-45); a bus having sets of data lines for connection to the arrays; circuitry to connect (controller 18) a regular array to either a first set or a second set of the data lines (Figure 4, data lines RAS_{1-n} and CAS_{1-n}), or to disconnect the regular array from the bus. Memory controller 18 controls the data lines connecting to the different memory banks (Column 3, lines 9-20).

Regarding Claims 7 and 12, Kronstadt discloses a memory 12 (Figure 4), comprising: a plurality of arrays of memory cells, the arrays being arranged in banks (banks 1 – n), each bank including regular arrays (array of static column mode dynamic random access memories, Column 2, lines 11-28), A.sub.0-N, and a redundant array (supports one or more redundant memory banks, Column 4, lines 25-45); a data bus having sets of N sets of bus lines, B.sub.0-N, for connection to the arrays (Figure 4, data lines RAS_{1-n} and CAS_{1-n}); logic associated with each array (controller 18), the logic being configured with a bit (valid field) that is set to a first state to

connect an ith regular array to an ith set of the bus lines, with the redundant array being disconnected from the data bus; a change in the bit setting from the first state to a second state (identifies invalid banks) causing the regular array, A.sub.i, to be disconnected from the data bus and the redundant array to be connected to the data bus. In instances where invalid banks are identified prior to an access, the access of an invalid bank is avoided. In this system, the invalid bank can be avoided by disabling the data line to such bank. In this case, the data line is not affected, but its connection to the invalid bank may be discontinued (Column 3, lines 15-45 and Column 4, lines 6-14). This is demonstrated by the instance in which banks are labeled invalid and a cache miss occurs until the banks are labeled valid again. The system avoids access to invalid banks.

Regarding Claims 2 and 13, Kronstadt discloses the memory of claim 1 wherein the circuitry (controller 18) comprises a bit (valid field) that, when set to a first logic state (identifies invalid banks), causes the circuitry to disconnect the regular array from the bus. In instances where invalid banks are identified prior to an access, the access of an invalid bank is avoided if possible. In this system, the invalid bank can be avoided by disabling the data line to such bank. In this case, the data line is not affected, but its connection to the invalid bank may be discontinued (Column 3, lines 15-45).

Regarding Claim 3, if the redundant bank is identified as a valid bank, such identification ("setting of the bit") can cause the controller to connect the redundant banks to a data line (See Figure 4).

Regarding Claims 4-5 and 9, the banks of Kronstadt et al. are arranged in a vertical linear configuration (See Figure 4) in which each banks is placed in one of multiple rows.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Kronstadt et al. (4,725,945) in view of Parulkar (6,769,081).

Regarding Claims 10 and 14, Kronstadt teaches the invention of Claims 7 and 12 above. The controller of Kronstadt et al. has circuitry to set a bit in accordance to the validity of a bank. However, Kronstadt does not teach setting the conductivity of a fuse to change the status of a bit. Parulkar discloses a programmable fuse used to set an address bit (Column 4, lines 30-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the bit of Kronstadt in the same manner as that of Parulkar because fuses are commonly found as components in computer systems and setting a fuse's conductivity is a quick and effective way to affect that value of a bit.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 11, 2005

Midys Inoa
Examiner
Art Unit 2189

MI

Pierre Vital
Primary Examiner
Art Unit 2188